Amendment to the Specification

Replace the paragraph under "RELATED APPLICATIONS" on page 1 with the following:

This application is a divisional application of United States Patent Application Serial No. 09/390,142 filed on September 3, 1999, which claims the benefit under 35 U.S.C. 120 to United States Patent Application Serial No. 09/261,112 filed 3 March 1999, and to United States Patent Application Serial No. 09/294,547 filed 19 April 1999, each of which ~~are~~ is hereby incorporated by reference.

Replace the paragraph starting at line 8 on page 1 with the following:

Modern integrated circuits have literally millions of active devices such as transistors and capacitors formed in or on a semiconductor substrate and rely upon an elaborate system of ~~metalization~~ metal layers, typically comprising multi-level ~~metalization~~ metal layers interconnections, in order to connect the active devices into functional circuits. An interlayer dielectric such as silicon dioxide is formed over a silicon substrate, and electrically isolates a first level of ~~metalization~~ metal layers which is typically aluminum from the active devices formed in the substrate. Metalized contacts electrically couple active devices formed in the substrate to the interconnections of the first level of ~~metalization~~ metal layers. In a similar manner, metal vias electrically couple interconnections of a second level of ~~metalization~~ metal layers to interconnections of the first level of ~~metalization~~ metal layers. Contacts and vias typically comprise a metal such as tungsten surrounded by a barrier metal such as titanium-nitride. Additional layers can be stacked to achieve the desired (multi-layer) interconnection structure.

Replace the paragraph starting at line 11 on page 2 with the following:

High density multilevel interconnections require the planarization of the individual layers of the interconnection structure and very little surface topography variation. Non-planar surfaces create poor optical resolution for the photo lithographic procedures used to lay done additional layers in later processing steps. Poor optical resolution prevents the printing of high density lines required for high density circuit and interconnect structures. Another problem associated with

surface topography variation pertains to the ability of subsequent ~~metalization~~ metal layers to cover or span the step height. If a step height is too large there is a potential danger that open circuits will be created causing failure of the chip on which the open circuit occurs. Planar interconnect surface layers are a must in the fabrication of ~~modern~~ state-of-the-art high density multilevel integrated circuits.

Replace the paragraph starting at line 16 on page 9 with the following:

FIG. 3 is a diagrammatic illustration showing a simple embodiment of the inventive two-chambered polishing head in FIG. ~~3~~ 2 further illustrating at exaggerated scale the manner in which linking elements (diaphragms) permit movement of the wafer subcarrier and wafer retaining ring.